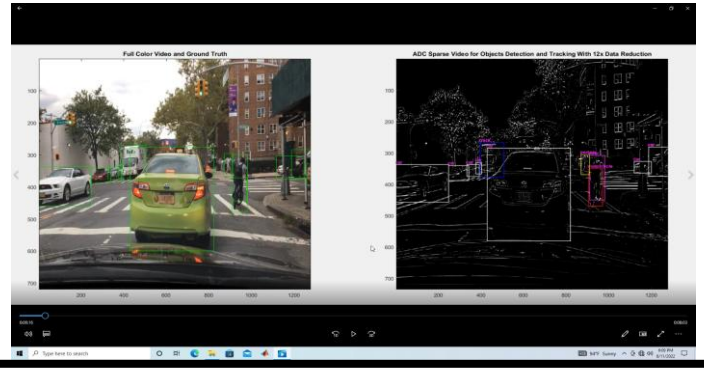
Adaptive Computation LLC (ADC)

Sparse Sensor, Hybrid In-Memory Processing Unit (HPU), Compiler Development, and Machine Intelligence Software applications

Tuan A Duong Ph.D.

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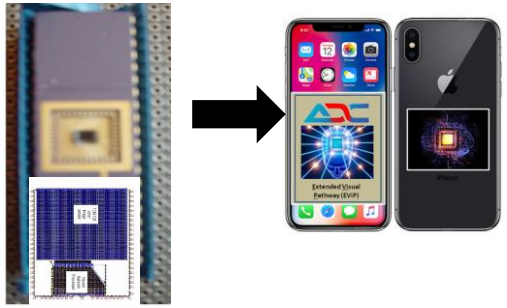
ADC Unique Innovations



- ✓ **Sparse Image (SI)**: lighter operations and low-cost space operation in visual data → 60x data reduction → military and space application markets

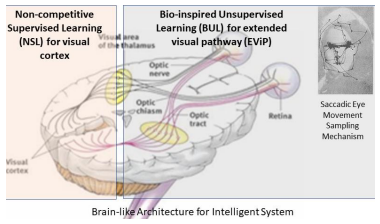
2 US patents DARPA support

- ✓ **Hybrid In-memory Processing Unit (HPU)**: fast processing, low power and compact device → over 3 orders of magnitude in faster speed processing and low power consumption → every application market required high speed and low power, e.g., mobile device
- ✓ **Massive Parallel Learning Architecture** (**MaPLA**): updating all weight components in fully parallel → enabling DNN learning time to be reduced from a week to an hour.
- ✓ **Compiler Development**: machine code operation → maximizing parallelism general purposed programming applications



US patent-Caltech Assignee Ongoing two provisional patents

- ✓ **Intelligent Software (IS)**: less data, in-situ data collection and learning → unattended and self-smart system → security, intelligent and exploration system



Brain-like Architecture for Intelligent System



TABLE I: HVIP VS EVIP COMPARISON BASED ON MEGAFACE CHALLENGE OF UOW

Distractors	1K-Rank1	10K-Rank1	10k-Rank 10
HViS*	75%	24%	91.1%
EViP	75%	66%	78.5%

3 US patents and 2 US international pending patents

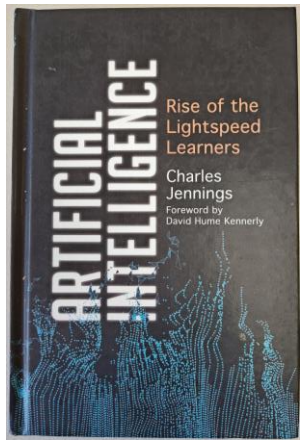
Integration of three will put us ahead of the game

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Credibility

Media:

- Book to experience and test with the ADC algorithm entitled “Artificial Intelligence: Rise of the Lightspeed Learners” by Charles Jennings, 2019 .

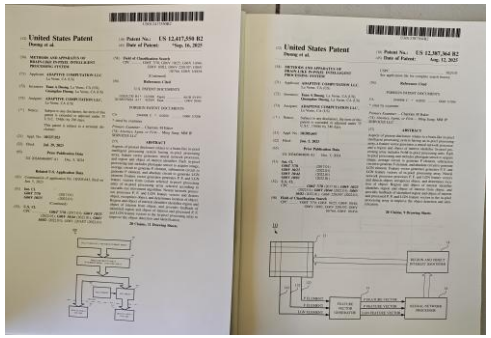


2025

- Press release 2025

https://www.prlog.org/13085112-bio-inspired-technology-dynamic-and-adaptable-for-unknown-real-world-environments.html

- a leading provider of bio-inspired AI technology aiming to tackle detecting and tracking elusive objects of interest across air, land, and space domains today announced that it has achieved “Awardable” status through DARPA Expedited Research Implementation Series (ERIS) Marketplace. The ERIS Marketplace is The DARPA Expedited Research Implementation Series (ERIS) Marketplace is a transformative digital platform designed to accelerate acquisition velocity and advance national security innovation, 2025.
- Selectable for sparse imager from AFWERX DP2 and in dialogue with DoD task.
- Negotiating the license of palm ID to a commercial start-up company for banking security
- Two patented US applications from the DARPA-AIE-IP2 Phase I and II tasks



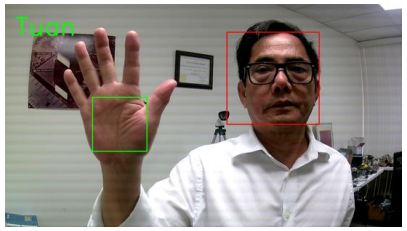


2026

- ***Press Release of June 4, 2026***

https://www.einpresswire.com/article/917194974/adaptive-computation-llc-assessed- and -awardable-for-darpa-eris-marketplace

- “Our solution “Real-Time Adaptive Tracking Systems for Irregular Target Moving Trajectory in a SWaP-C Approach”has been competitively assessed by the Defense Advanced Research Projects Agency (DARPA) and has been deemed “awardable” in the Expedited Research Innovation System (ERIS) Marketplace, making it available to view and easily procurable by the Department of War.”
- Complete software and hardware for Face/Palm ID and commercial partner is evaluating it.



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Competitive Landscape in AI Processor

ADC's HPU Engine

Hardware

- Analog input and digital weight
- Full Parralel In memory Computing- Instant Access
- Multiplication and accumulation in parallel
- Fully parallel access from sensory analog data
  - **8-bit accuracy**

Software

- Proven bio-inspired unsupervised learning based on extended visual pathways (EViP) as short-term memory operation
- Dynamic supervised learning as brain-based learning features: no constraints in data arrival and self-managed new class as long-term memory

  → **Autonomous and self-intelligence at the edge**

Fast, low-power, and user-friendly engine and intelligence enabling approach

Nvidia GPU Engine

Hardware

- Digital / Digital
- Sequential Von-Neumann Architecture- moving data out from memory for computing
- Multiplication, addition and accumulation in sequential
- Sequential data assessment from sensory digital data
  - **32- or 64-bit accuracy**

Software

- CUDA library to enable parallelism of computation
- Deep learning-based architectures for a statistical learning approach; hence, no intelligence system is enabled

→ **No autonomous and manned managed intelligence**

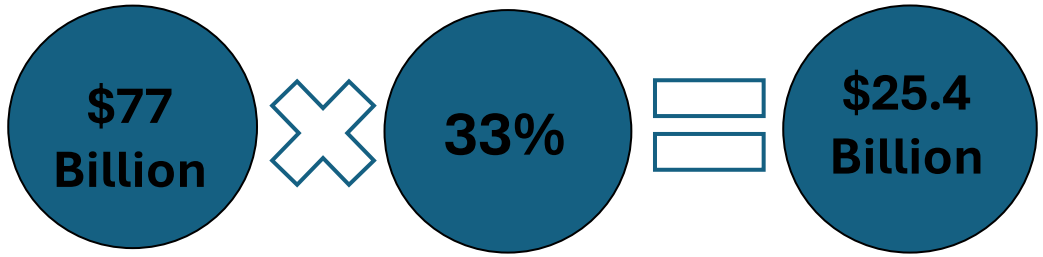
Slow, Power hungry and not user-friendly engine and no intelligence enabling

Co-Design software and hardware enables impeccable and unique products in the modern AI era.

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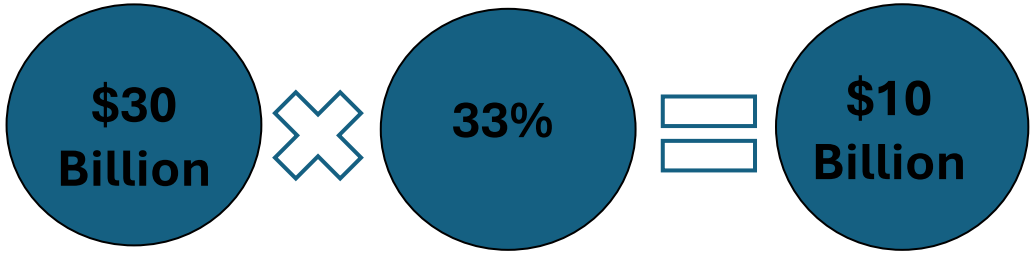
Market Size

AI Hardware



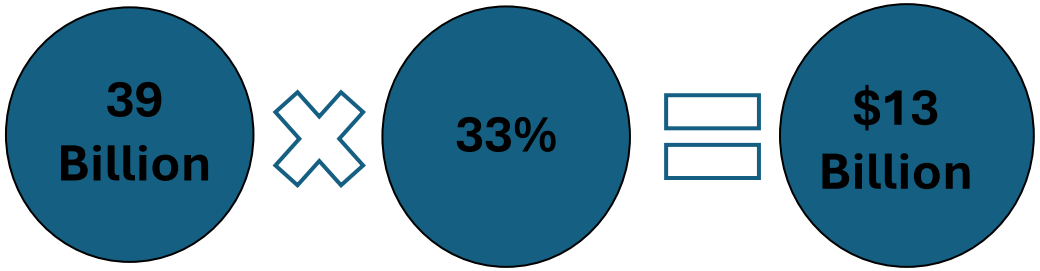
Market in 2027 | 33% for net revenue | ADC annual ecosystem

AI Edge Hardware



Co-processor Sales as OEM | 30$ /co-processor system and 33% for net revenue | ADC annual ecosystem

Camera Sensor



Market in 2027 | 33% for net revenue | ADC annual ecosystem

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Team

Dr. Tuan Duong – CEO and CTO

- 26 of year Neural Network S/H-Ware veteran at NASA and 15 years at ADC
- Holds 20 patents (Caltech/NASA and ADC) and 30 NASA New Technology Reports
- Passion and innovative in neural networks for ‘true’ intelligent

Dr. Nam Trang– Data Science Manager

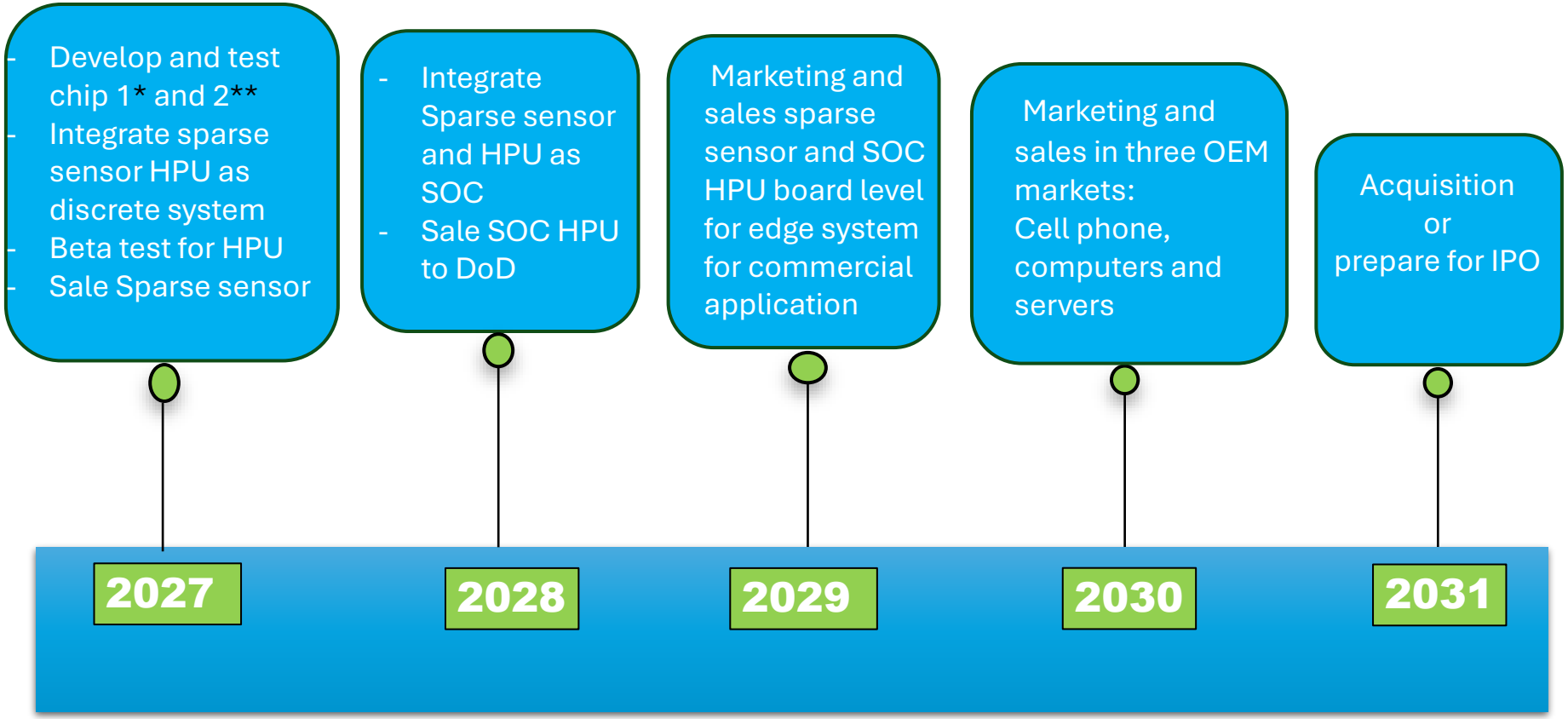
- Ph.D. UC Berkeley
- Several NSF Career grants
- Young and full energy for challenging tasks.

Dr. Allen R. Stubberud- VP-Advisor

- Dean and Prof. at UCI
- Former Chief scientist of Air Force
- Experienced and wisdom.

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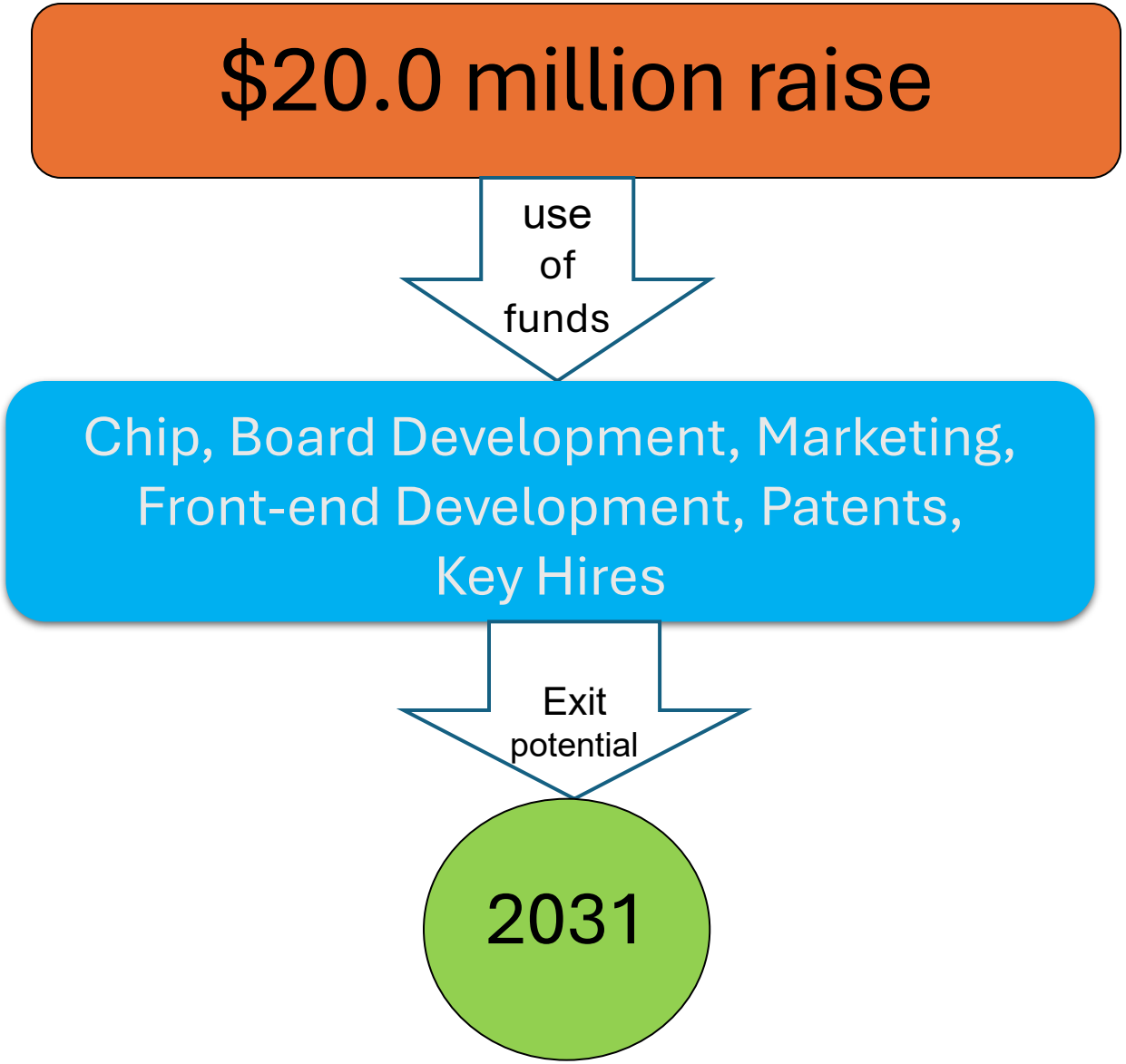
MILESTONES



* Sparse sensor
** Hybrid In-memory Processing Unit (HIPU)

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ASK



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Background

(all these works are done in-memory architecture)

NASA

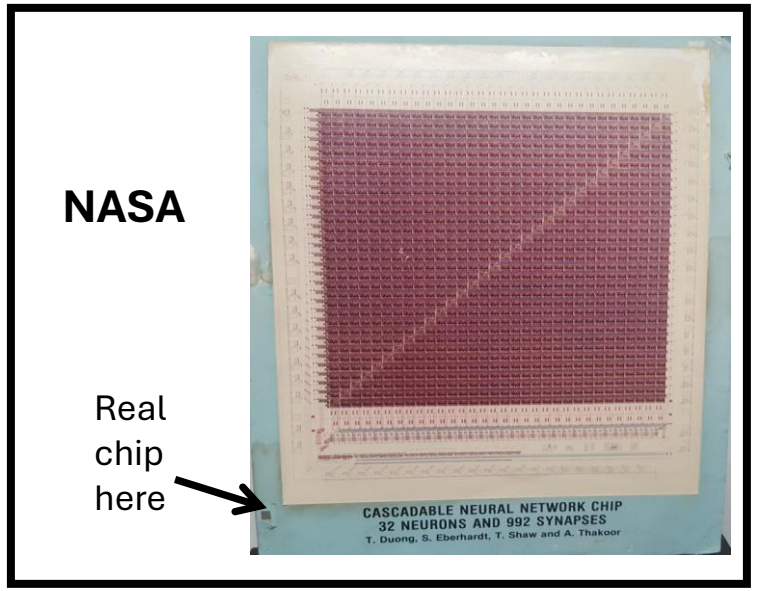
- **Year 1990**- Successfully developed and tested 992 synapse array and 32 neurons Neural Network chip for associative memory using neural network feedback mode.
- **Year 1994**- Modified version of 1990 neural network chip successfully launched on STRV-1b to study on-chip learning capability to adapt the total dose in the radiation environment- the first neural network chip flew to space—NASA task.

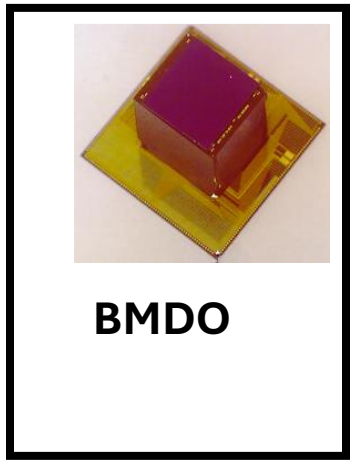
DOE

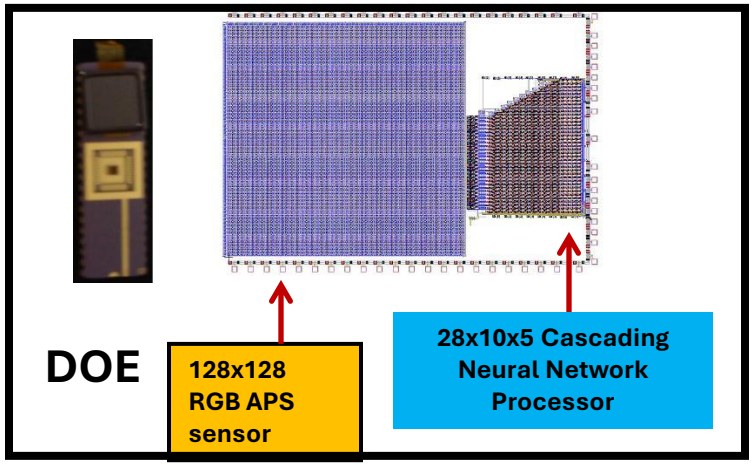
- **Year 2000**- Successfully developed and tested 128x128 RGB color array and 28x10x5 cascade neural network processor on a chip (Soc) for DOE task as subcontractor for IOS.

BMDO

- Year 1997- Successfully developed and tested a chip level for 3-D stacking chip (64x64x64 8-bit synapse array)

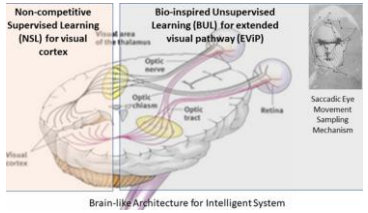






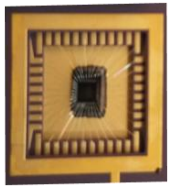
Dr. Duong (who was the first to work on in-memory processing 30 years ago) was the cognitive architect and engineer for these projects and successfully wrote the learning software for the first neural network chip flow into space

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Brain-like Architecture for Intelligent System

ADC TECHNOLOGY INNOVATIONS



ViCFA Software — Brain like Learning as long-term memory

Adapted the learning object without competition in natural mode, **Vi**sual **C**ortex **F**unction **A**pproximation (ViCFA) is initiated and developed to achieve:

- Fast learning
- Sequential Learning as data available—No redo learning
- No constraints in sample data
- Universal optimal architecture
- Autonomy

Basic Benchmarks are validated and advanced in fast, on-line, and autonomous learning, to meet the intelligence at the edge processing.

2 Pending patent
International patent

EViP Software—Brain-like Extraction image as short-term memory

Inspired by the mammalian visual system, ADC integrates a saccadic eye movement emulator with a model of the biological visual pathway, namely **E**xtended **Vi**sual **P**athway (**EViP**) to enable real-time processing for the detection and recognition of a single-glance-on-object database, given inputs that are:

- partial-view or full-view
- low resolution or "noisy"
- incomplete or "collage" style
- sketches of actual objects

3 US patents

Benchmark tests show this system **exceeds human visual performance** in "Rank 1" recognition tests with the *same single-glance-on-object database* .

Hybrid Processor Unit and sparse Imager:

Analog + digital on one chip enables:

- low power and optimal computation
- parallel computation→ high speed
- compact architecture

Revolutionary digitally-refined analog architecture puts "the best of both worlds" on a single chip, providing high speed, high performance, and low power consumption in a device that fits in smart phone slot.

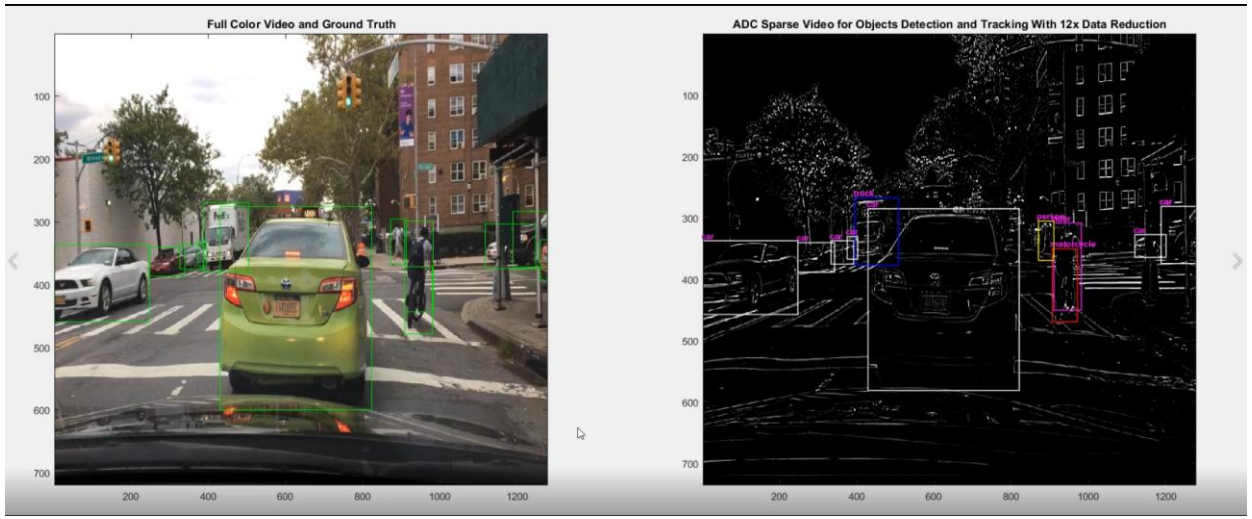
2 US Patents

The brain-like Intelligent System (BIS) combination of software and hardware will provide unique advantages in technology for machine intelligence, perception and cognition, especially for handheld and edge computing applications.

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AIE DARPA IP2 Program Results (Phase I and II)

AIE is ai exploration program in third wave (while Deep Learning is a second wave) in Defense advanced research program agency (DARPA)-the revolutionary research program in us



Sparse sensor using ADC-extended visual pathway (EViP)* patented by ADC, to provide sufficient information as equivalent to full color sensor, to harvest low power consumption and fast computation due to much less data (60x reduction).

Who cares?
Drone, Edge system, space commercial and military applications.

* Tuan A. Duong, Vu A. Duong and Allen R. Stubberud, “Shape and Color Features for Object Recognition Search,” Handbook of Pattern Recognition and Computer Vision, Chap. 1.5, Ed. C.H. Chen, 4th Edition by World Scientific Publishing Co. Pte. Ltd, Jan 2010.

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Hybrid In-memory Processing Unit (HPU)—opportunity

- Define the AI hardware market with the innovative approach.
- Set a cornerstone in the AI landscape in the future, specially for edge and space applications.
- Open the door for self-training data generation and self-learning for exploratory mission in space with ADC software approach.

Nvidia is dominating in AI GPU processors, but the technology is drawback by using Von Neumann architecture and digital information.

This opens a new direction for in-memory computing (DARPA is heading now) and a hybrid approach.

Dr. Duong has been working on this approach* for over 30 years, and we flew a learning device in space to adapt to the radiation environment in STRV-B in 1994. He holds the key technologies in hardware and software.

* Tuan A. Duong, S. Kemeny, T. Daud, A. Thakoor, C. Saunders, and J. Carson, "Analog 3-D Neuro-processor for Fast Frame Focal Plane Image Processing," The Industrial Electronics Handbook, Chap. 73, Ed.-In-Chief J. David Irwin, CRC PRESS, 1997.
* Tuan A. Duong, S.P. Eberhardt, T. Daud, and A. Thakoor, "Learning in neural networks: VLSI implementation strategies," In: Fuzzy logic and Neural Network Handbook, Chap. 27, Ed: C.H. Chen, McGraw-Hill, 1996.

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COMPETITIVE LANDSCAPE IN SENSORY DATA

ADC proved that sparse data using EViP which is reduced 60x intensity data is equivalent full resolution



Sparse data requires less computation; hence it enables fast and low power requirements

Current Practice

Full color image is used



Abundant data requires more computation to produce slow and power-hungry demands

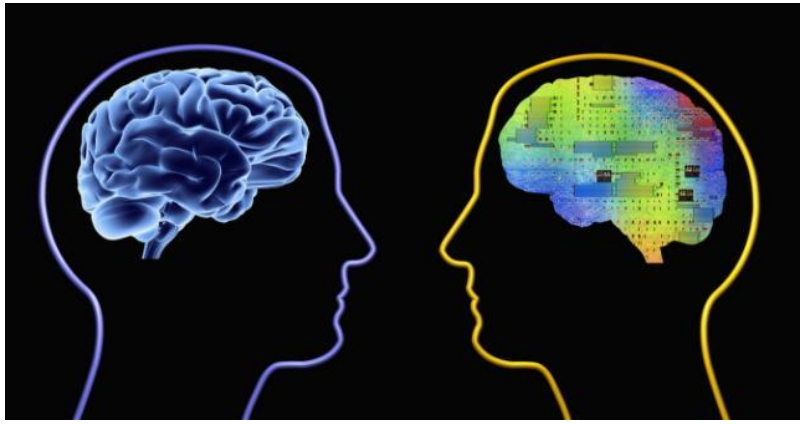
ADC brings new technology sparse data using EViP to define a new sensory data direction for future use.

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Human Visual System (HViS) vs. Extended Visual Pathway (EViP)-HIP

- For a single-sample database, detailed testing has shown that ADC's EViP system can match human visual system performance (75% correct) in a face recognition task involving a database with 1,000 distractors. With 10,000 distractors, **EViP *outperforms* HViS**, providing 66% versus 24% correct recognition in rank 1. However, HViS is still more flexible and versatile to outperform EViP in rank 10.

  *http://megaface.cs.washington.edu/results/humanstudy.html

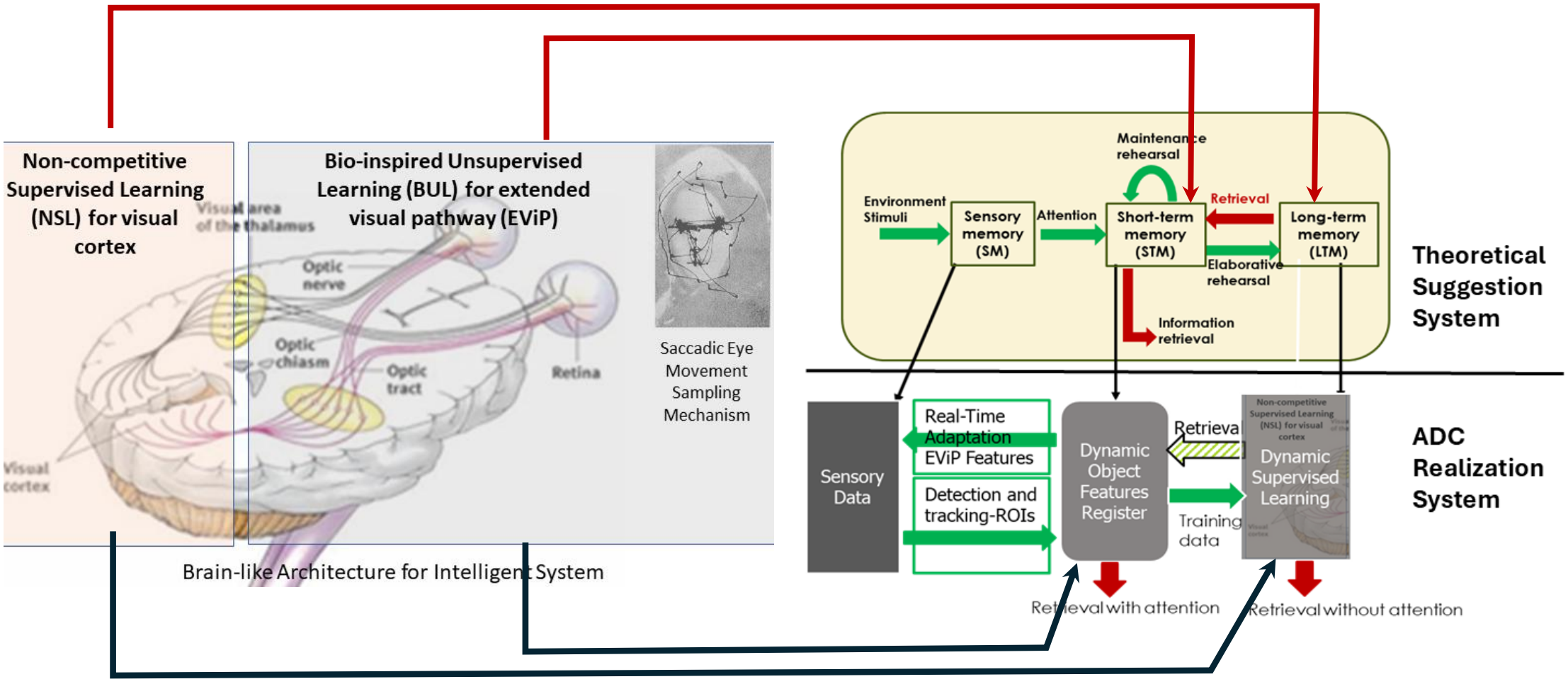


Distractors	1K-Rank1	10K-Rank1	10k-Rank 10
HViS*	75%	24%	91.1%
EViP	75%	66%	78.5%

This technology is recognized as a new AI direction in the book entitled "**Artificial Intelligence: Rise of the Lightspeed Learners**" by Charles Jennings. (https://www.amazon.com/Artificial-Intelligence-Rise-Lightspeed-Learners/dp/1538116804).

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Neuroscience Architecture



Market Estimation for AI Hardware

According to Global Market Insights Inc. (GMI), the global AI Hardware market size was estimated at USD 59.3 billion in 2024. The market is expected to grow from USD 66.8 billion in 2025 to USD 296.3 billion in 2034, at a CAGR of 18%. https://www.gminsights.com/industry-analysis/ai-hardware-market?utm_source=chatgpt.com

Investment in Edge AI hardware

The global edge artificial intelligence chips market size was valued at USD 3 billion in 2024 and is estimated to grow at 24.8% CAGR from 2025 to 2034. The growth of the market is attributed to the increasing demand for semiconductors and the increase in the adoption of IoT technologies. (https://www.gminsights.com/industry-analysis/edge-artificial-intelligence-chips-market?utm_source=chatgpt.com)

Market Estimation for Image Sensor Market

The Image Sensor Market size is projected to reach USD 38.6 billion by 2027 from an estimated USD 26.1 billion in 2022 at a CAGR of 8,1% from 2022 to 2027.
https://www.marketsandmarkets.com/Market-Reports/Image-Sensor-Semiconductor-Market-601.html

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Go to Market

PR/Marketing

- Tech show
- Electronic consumer third parties
- Tech magazines
- Google/Facebook ads
- Retail co-marketing
- Affiliate programs

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Product Timing Projection

Software

•All software in supervised and unsupervised learning are developed.

•Unsupervised Learning is optimized

•Supervised is under optimized

•Integration is on going

Hardware

•Chip architecture is well-defined

• Component designs are initiated

	Estimated ready in	What we need
Chip Development and Test Board application Development	Stage 1:6 months Stage 2: 7:12 months	Develop, test, integration and marketing
Chip optimization and test Board application Development	13-15 months Stage 3: 16-19 months	Fine-tune, test, integration Marketing team
OEM ready for Edge device, Phone, Computers and Servers	19-48 months	Marketing for sales
New chip submission (lower sub-micron technology)	25-30 months	New chip version ready
Product upgrade and IPO	49-60 months	IPO or Acquisition

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FINANCIALS

	Year 1	Year 2	Year 3	Year 4	Year 5
Sales Revenue	$250,000	$1,500,000	$40M	$250M	$1B
Operating Expense	6,000,000	10,500,000	35M	50M	200M
EBITDA	(5,750,000)	(9,000,000)	5M	200M	800M
Series A	20M				
Series B			50M		

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Competitions

- Mythic: Builds an Analog Processing Unit (APU) using analog compute-in-memory for high-efficiency edge AI and automotive vision.

Problems: 8-bit sub-threshold analog levels is challenges due to processing variations and mirrors, no on-chip learning

- **TetraMem**: Develops multi-level RRAM (Resistive RAM) in-memory computing SoCs to accelerate neural network inference.

Problems: Extra processes and processing variations, no on-chip learning

- **Axelera AI**: Produces edge AI chips utilizing in-memory computing architectures.

Problems: uses a highly optimized digital hardware matrix acceleration strategy, hence power hungry, no on-chip learning

Optimization software and download weight sets-No on-chip learning

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ADC, Caltech, and NASA Ips for neural networks

1. US patent, "Cascaded VLSI Chips for On-line Learning," by T. A. Duong, T. Daud, and A. Thakoor; Patent No. A5,479,579 (**NASA Assignee**).
2. US patent, "Input Circuit for an Image Processor" by T. A. Duong, Patent No. 6,307,587, Issued: 10/ 23/2001 (**Caltech Assignee**)
3. US patent, "On-chip learning in VLSI hardware," by T. A. Duong, Patent No 6,513,023 Issued: 01/28/2003 (**NASA Assignee**).
4. US patent, "Artificial Intelligence Systems for Identifying Objects," T. A. Duong, V. A. Duong and Allen R. Stubberud, Patent Number: 7,711,157 Issued: 5/4/2010 (**Caltech Assignee**).
5. US Patent, "System and Method for Cognitive Processing for Data Fusion," T. A. Duong and V. A. Duong, Patent # 8,204,927 B1, Issued: June 19, 2012 (**Caltech Assignee**).
6. US patent, "Optimal Dynamic Sub-Threshold Technique for Extreme Low Power Consumption for VLSI," T. A. Duong, Patent # US-2012-0206188-A1, Issued: August 16, 2012 (**Caltech Assignee**).
7. US Patent, "Method and System for Object Recognition Search," T. A. Duong, V. A. Duong and A. R. Stubberud, Patent No. 8340435, Issue Date Dec. 25, 2012 (**Caltech Assignee**).
8. US patent, " Compressive Sensing based Bio-Inspired Shape Feature Detection CMOS Imager," T. A. Duong, Patent No. 8,976,269, Issue Date March 10, 2015 (**Caltech Assignee**).
9. US patent, "Image Integration Search Based on Human Visual Pathway Model," Tuan A Duong, Patent No. 9,846,808, Issue Date December 19, 2017 (**ADC Assignee**).
10. US patent, "Systems and methods for object recognition based on human visual pathway", Tuan A Duong, Patent No 10133955, Patent date Issued Nov 20, 2018 (**ADC Assignee**)
11. US patent, "Image Integration Search Based on Human Visual Pathway Model," Tuan A Duong, Patent No. 9,846,808, Issue Date May 16, 2019 (**ADC Assignee**).
12. US Patent, "Methods and Apparatus of Brain-like In-pixel Intelligent Processing Systems", US 12387364 B2, T.A. Duong and QD. Duong, Aug 12, 2025 (**ADC Assignee**).
13. US Patent, "Methods and Apparatus of Brain-like In-pixel Intelligent Processing Systems-Architecture," US12417550 B2, T.A. Duong and QD. Duong, Sept. 16, 2025. (**ADC Assignee**).
14. International patent WO 2024/145079 A1, "Dynamic Neural Distribution Function Machine Learning Architecture," Issued July 04, 2024 (**ADC Assignee**).
15. US Patent, "Dynamic Neural Distribution Function Machine Learning Architecture," US 2024/0220788 A1, T.A. Duong and QN. Duong, July 4, 2024. (**ADC Assignee**).
16. US Pending, " Dynamic Supervised Neural Distribution Function Learning Systems," US-patent Application 19/560015, T.A. Duong and QN. Duong, March 7, 2026 (**ADC Assignee**).
17. US Provisional Patent: "Hybrid 8-Bit Accuracy Precision Synaptic Weight for In-Memory Processing Architecture," T.A. Duong and QD. Duong, ADC-0001-P1, A#64/147019, filed Sept. 2, 2026.
18. US Provisional Patent: "Massively Parallel Learning in VLSI Hardware," T.A. Duong and QD. Duong, ADC-0001-P2, A#64/147007, filed Sept. 2, 2026.

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